

Low Voltage/Low Power CMOS 16-bit Microcontroller TMP91PW11F

1. Outline and Device Characteristics

The TMP91PW11 is OTP type MCU which includes 128 Kbyte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP91CW11 by general EPROM programmer.

The TMP91PW11 has the same pin-assignment as the TMP91CW11 (Mask ROM type).

Writing the program to Built-in PROM, the TMP91PW11 operates as the same way as the TMP91CW11.

MCU	ROM	RAM	Package	Adapter Socket
TMP91PW11F	OTP 128 Kbyte	4 Kbyte	P-LQFP100-1414-0.50C	BM11129

000707EBP1

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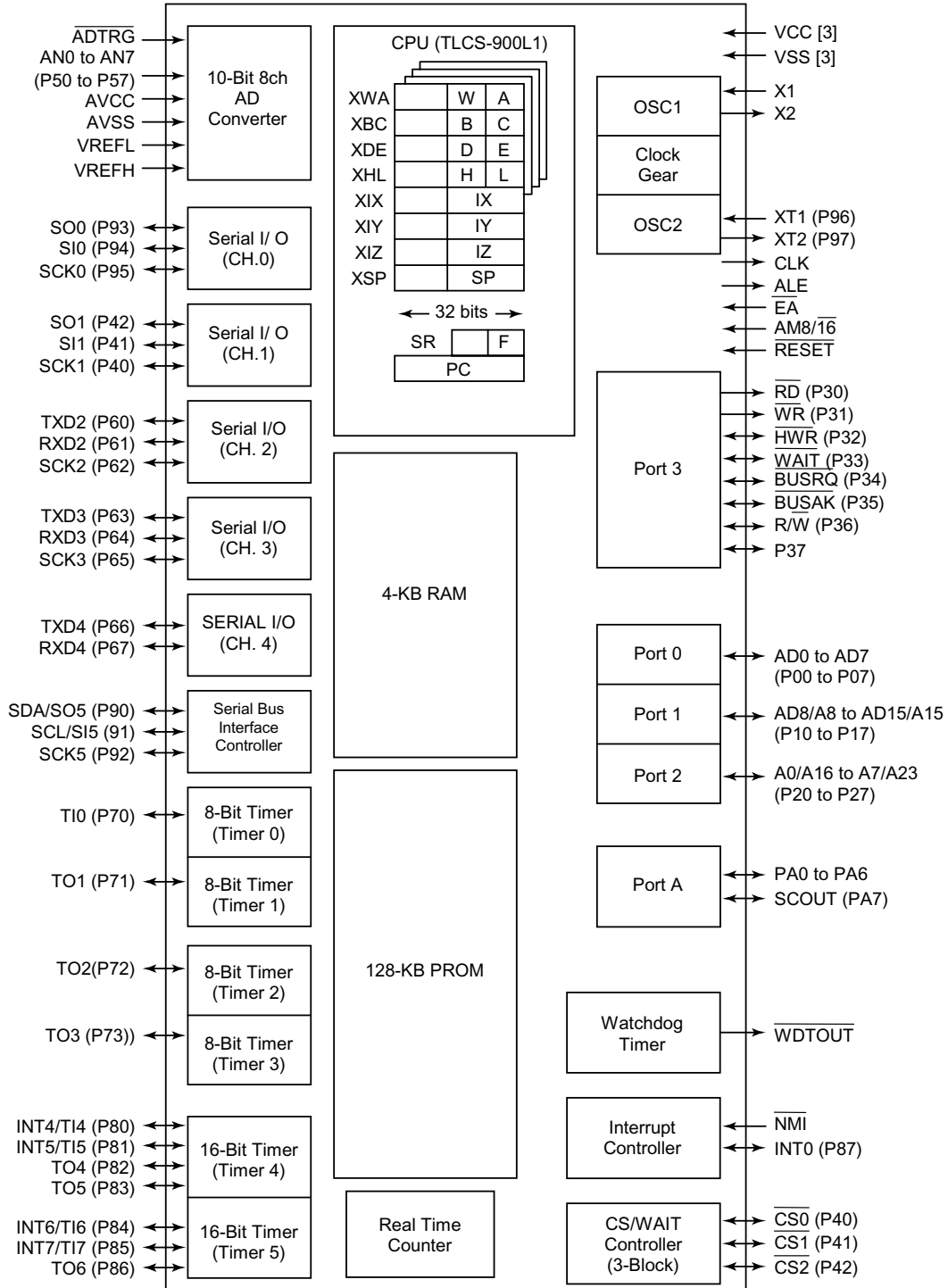


Figure 1.1 TMP91PW11 block diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91PW11F, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of TMP91PW11F.

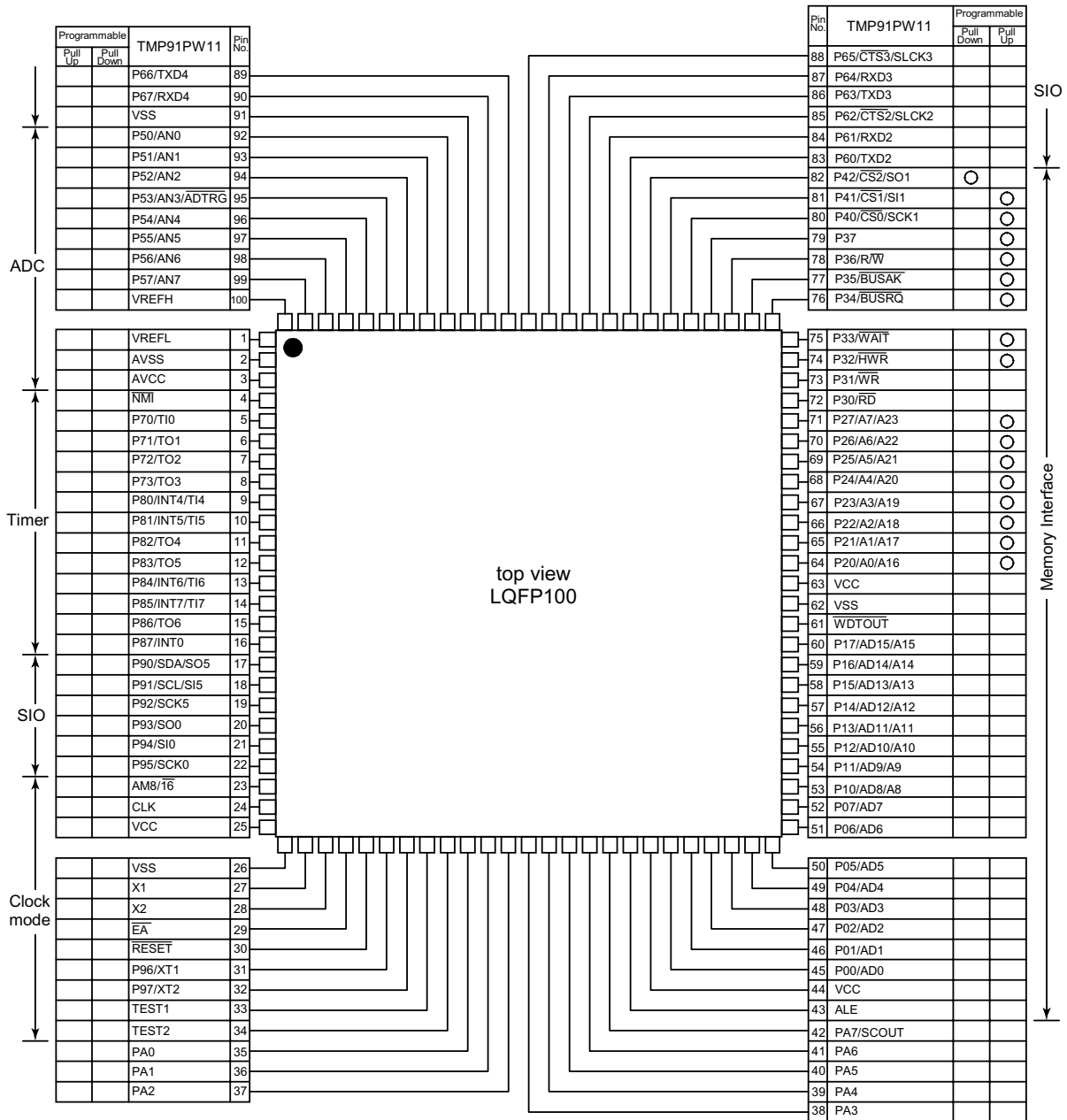


Figure 2.1.1 Pin assignment

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/4)

Pin name	Number of pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows selection of I/O on a bit basis Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 \overline{RD}	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 \overline{WR}	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 \overline{HWR}	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 \overline{WAIT}	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 \overline{BUSRQ}	1	I/O Input	Port34: I/O port(with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0-23, \overline{RD} , \overline{WR} , \overline{HWR} , R/\overline{W} , \overline{RAS} , $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 \overline{BUSAK}	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, \overline{RD} , \overline{WR} , \overline{HWR} , R/\overline{W} , \overline{RAS} , $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving \overline{BUSRQ} . (For external DMAC)
P36 $\overline{R/\overline{W}}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$ SCK1	1	I/O Output I/O	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Serial clock I/O 1

Note: This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller, using the \overline{BUSRQ} and \overline{BUSAK} signals.

Table 2.2.2 Pin names and functions (2/4)

Pin name	Number of pins	I/O	Function
P41 CS1 SI1	1	I/O Output Input	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Serial receive data 1
P42 CS2 SO1	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Serial send data 1
P50 to P52 AN0 to AN7	3	Input Input	Port5: Input port Analog input: Analog signal input for AD converter
P53 AN3 ADTRG	1	Input Input Input	Port 53: Input Port Analog input = Analog signal input for AD converter AD external trigger
P54 to P57 AN4 to AN7	4	Input Input	Port 5: Input Port Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port (Programmable open drain) Serial send data 2
P61 RXD2	1	I/O Input	Port 61: I/O port Serial receive data 2
P62 CTS2 SCLK2	1	I/O Input I/O	Port 62: I/O port serial data send enable 2 (Clear To Send) Serial Clock I/O 2
P63 TXD3	1	I/O Output	Port 63: I/O port Serial send data 3
P64 RXD3	1	I/O Input	Port 64: I/O port Serial receive data 3
P65 CTS3 SCLK3	1	I/O Input I/O	Port 65: I/O port Serial data send enable 3 (Clear To Send) Serial Clock I/O 3
P66 TXD4	1	I/O Output	Port 66: I/O port Serial send data 4
P67 RXD4	1	I/O Input	Port 67: I/O port Serial receive data 4
P70 TI0	1	I/O Input	Port 70: I/O port Timer input 0: timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port PWM output 3: 8-bit PWM timer 3 output

Table 2.2.3 Pin names and functions (3/4)

Pin name	Number of pins	I/O	Function
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port Timer output 5: Timer 4 output pin
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 SDA SO5	1	I/O I/O Output	Port 90: I/O port (Programmable open-drain) SBI I ² C bus mode channel data Serial send data 5
P91 SCL SI5	1	I/O I/O Input	Port 91: I/O port (Programmable open drain) SBI I ² C bus mode clock Serial receive data 5
P92 SCK5	1	I/O I/O	Port 92: I/O port Serial Clock I/O 5
P93 SO0	1	I/O Output	Port 93: I/O port (Programmable open drain) Serial send data 0
P94 SI0	1	I/O Input	Port 94: I/O port Serial receive data 0
P95 SCK0	1	I/O I/O	Port 95: I/O port Serial clock I/O 0
PA0 to PA5	6	I/O	Port A0 to A5: I/O ports (large current output)
PA6	1	I/O	Port A6: I/O port

Table 2.2.4 Pin names and functions (4/4)

Pin name	Number of pins	I/O	Function
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs system clock or 2 times oscillation clock for synchronizing to external circuit.
WD $\overline{\text{TOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs [System Clock \div 2] Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	Fixed to 1.
AM8/ $\overline{\text{16}}$	1	Input	Fixed to 1.
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1	1	Input	Low Frequency Oscillator connecting pin
P96		I/O	Port 96: I/O port (Open Drain Output)
XT2	1	Output	Low Frequency Oscillator connecting pin
P97		I/O	Port 97: I/O port (Open Drain Output)
TEST1/TEST2	2	Output /Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin (All VCC pins are connected to the power supply source.)
VSS	3		GND pin (All Vss pins are connected to the GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: Built-in pull-up/pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

2.3 PROM mode

Table 2.3.1 Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{\text{CE}}$	1	Input	Chip enable	P32
$\overline{\text{OE}}$	1	Input	Output enable	P30
PGM	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	$\overline{\text{EA}}$
VCC	4	Power supply	6.25 V/5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS
Pin function	Number of pins	Input / Output	Pin state	
P34	1	Input	Fix to low level (security pin)	
$\overline{\text{RESET}}$	1	Input	Fix to low level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Self oscillation with resonator	
X2	1	Output		
P42 to P40 P37 to P35 AM8/ $\overline{16}$	7	Input	Fix to high level	
TEST1/TEST2	2	Input / Output	Short	
P57 to P50 P67 to P60 P73 to P70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{\text{NMI}}$ WDTOU $\overline{\text{T}}$	48	I/O	Open	

3. Operation

This section describes the functions and basic operational blocks of the TMP91PW11.

The TMP91PW11 has PROM in place of the mask ROM which is included in the TMP91CW11. The other configuration and functions are the same as the TMP91CW11. Regarding the function of the TMP91PW11, which is not described herein, see the TMP91CW11.

The TMP91PW11 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by releasing the CLK pin (Pin open). In the MCU mode, the operation is the same as TMP91CW11.

(2) Memory-map

The memory map of TMP91PW11 is the same as that of TMP91CW11. The memory map in MCU mode and the memory map in PROM mode are shown in Figure 3.2.1.

3.2 Memory Map

Figure 3.2.1 are the memory map of the TMP91PW11.

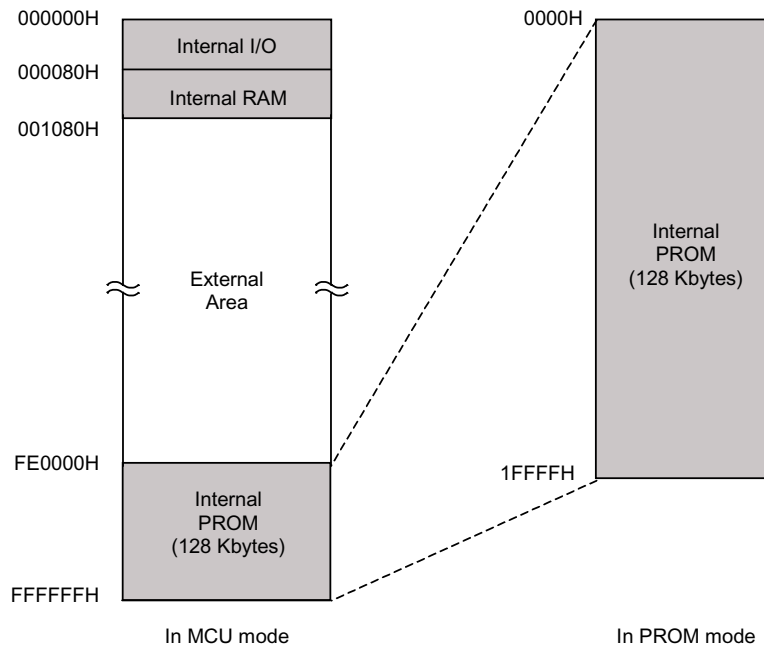


Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

X used in an expression shows a frequency of clock f_{PPH} selected by SYSCR1 <SYSCK>. If a clock gear or a low speed oscillator is selected, a value of X is different. The value as an example is calculated at f_c , gear = 1/ f_c (SYSCR1 <SYSCK, GEAR 2 to 0> = 0000).

Parameter	Symbol	Pin	Rating	Unit
Power Supply voltage	V_{CC}		-0.5 to 6.5	V
Program voltage	U_{PP}	$\bar{E}A$	-0.5 to 13.0	V
Input Voltage	V_{IN}		-0.5 to $V_{CC} + 0.5$	V
Output Voltage	V_{OUT}	P96, P97, PA0 to A5, P60, P91 to 93 (for open-drain)	-0.5 to $V_{CC} + 0.5$	V
Output Current (per pin)	I_{OUT1}	only PA0 to A5	20	mA
	I_{OUT2}	except PA0 to A5	2	mA
	I_{OUT3}		-2	mA
Output Current (total)	ΣI_{OUT1}	Total	120	mA
	ΣI_{OUT2}	PA0 to A5	80	mA
	ΣI_{OUT3}	Total	-80	mA
Power Dissipation ($T_a = 85^\circ\text{C}$)	P_D		600	mW
Soldering Temperature	T_{solder}		260	$^\circ\text{C}$
Storage Temperature	T_{STG}		-65 to 150	$^\circ\text{C}$
Operating Temperature	T_{opr}		-40 to 85	$^\circ\text{C}$

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2) ($V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }85^\circ\text{C}$)

Parameter		Symbol	Condition		Min	Typ. (Note 1)	Max	Unit	
Power Supply Voltage $AV_{CC} = V_{CC}$ $AV_{SS} = V_{SS}$		VCC	fc = 4 to 25 MHz	fs = 30 to 34 kHz	4.5		5.5	V	
			fc = 4 to 12.5 MHz		2.7				
Input Low Voltage	AD0 to 15	VIL	$V_{CC} \geq 4.5\text{ V}$		-0.3		0.8	V	
			$V_{CC} < 4.5\text{ V}$				0.6		
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VI1	$V_{CC} = 2.7\text{ to }5.5\text{ V}$				0.3 V_{CC}		
		$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P40 to 41, P87, P90 to 92, P94, P95					VI2		0.25 V_{CC}
		$\overline{\text{EA}}$, AM8/16					VI3		0.3
		X1					VI4		0.2 V_{CC}
Input High Voltage	AD0 to 15	VIH	$V_{CC} \geq 4.5\text{ V}$		2.2	$V_{CC} + 0.3$			
			$V_{CC} < 4.5\text{ V}$		2.0				
	P20 to 27, P32 to 37, P42, P50 to 57, P60 to 67, P70 to 73, P80 to 86, P93, P96, P97 to 37, PA0 to A7	VIH1	$V_{CC} = 2.7\text{ to }5.5\text{ V}$		0.7 V_{CC}				
		$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P40 to 41, P87, P90 to 92, P94, P95			VIH2		0.75 V_{CC}		
		$\overline{\text{EA}}$, AM8/16			VIH3		$V_{CC} - 0.3$		
		X1			VIH4		0.8 V_{CC}		

Note: Typical values are for $T_a = 25^\circ\text{C}$ and $V_{CC} = 5\text{ V}$ unless other wise noted.

4.2 DC Characteristic (2/2) ($V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }85^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output Low Voltage (except PA0 to PA5)	V_{OL}	$I_{OL} = 1.6\text{ mA}$ ($V_{CC} = 2.7\text{ to }5.5\text{ V}$)			0.45	V
Output Low Current (PA0 to 5)	I_{OLA}	$V_{OL} = 1.0\text{ V}$ ($V_{CC} = 3\text{ V} \pm 10\%$)	7			mA
		$V_{OL} = 1.0\text{ V}$ ($V_{CC} = 5\text{ V} \pm 10\%$)	16			
Output High Voltage	V_{OH1}	$I_{OH} = -400\text{ }\mu\text{A}$ ($V_{CC} = 3\text{ V} \pm 10\%$)	2.4			V
	V_{OH2}	$I_{OH} = -400\text{ }\mu\text{A}$ ($V_{CC} = 5\text{ V} \pm 10\%$)	4.2			
Darlington Drive Current (8 Output Pins max.)	I_{DAR} (Note 2)	$V_{EXT} = 1.5\text{ V}$ $R_{EXT} = 1.1\text{ k}\Omega$ ($V_{CC} = 5\text{ V} \pm 10\%$ only)	-1.0		-3.5	mA
Input Leakage Current	I_{LI}	$0.0 \leq V_{IN} \leq V_{CC}$		0.02	± 5	μA
Output Leakage Current	I_{LO}	$0.2 \leq V_{IN} \leq V_{CC} - 0.2$		0.05	± 10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	$V_{IL2} = 0.2 V_{CC}$, $V_{IH2} = 0.8 V_{CC}$	2.0		6.0	V
$\overline{\text{RESET}}$ Pull Up Resistor	R_{RST}	$V_{CC} = 5\text{ V} \pm 10\%$	50		150	k Ω
		$V_{CC} = 3\text{ V} \pm 10\%$	80		200	
Pin Capacitance	C_{IO}	$f_c = 1\text{ MHz}$			10	pF
Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P40, P41, P87, P90 to 92, P94, P95	V_{TH}		0.4	1.0		V
Programmable Pull Down Resistor	R_{KL}	$V_{CC} = 5\text{ V} \pm 10\%$	10		80	k Ω
		$V_{CC} = 3\text{ V} \pm 10\%$	30		150	
Programmable Pull Up Resistor	R_{KH}	$V_{CC} = 5\text{ V} \pm 10\%$	50		150	k Ω
		$V_{CC} = 3\text{ V} \pm 10\%$	100		300	
NORMAL	I_{CC}	$V_{CC} = 5\text{ V} \pm 10\%$ $f_c = 25\text{ MHz}$		45	55	mA
RUN				30	40	
IDLE2				18	30	
IDLE1				3.5	10	
NORMAL	I_{CC}	$V_{CC} = 3\text{ V} \pm 10\%$ $f_c = 12.5\text{ MHz}$ (Typ: $V_{CC} = 3.0\text{ V}$)		13	20	mA
RUN				8	11	
IDLE2				4.8	7.5	
IDLE1				1.1	1.8	
SLOW	I_{CC}	$V_{CC} = 3\text{ V} \pm 10\%$ $f_s = 32.768\text{ kHz}$ (Typ.: $V_{CC} = 3.0\text{ V}$)		110	200	μA
RUN				30	52	
IDLE2				25	52	
IDLE1				15	40	
STOP		$V_{CC} = 2.7\text{ to }5.5\text{ V}$	$T_a \leq 50^\circ\text{C}$	0.2	10	μA
			$T_a \leq 70^\circ\text{C}$		20	
			$T_a \leq 85^\circ\text{C}$		50	

Note 1: Typical values are for $T_a = 25^\circ\text{C}$ and $V_{CC} = 5\text{ V}$ unless otherwise noted.

Note 2: I-DAR is guaranteed for total of up to 8 ports.

4.3 AC Characteristics

- (1) $V_{CC} = 5\text{ V} \pm 10\%$ ($f_c = 4\text{ to }20\text{ MHz}$)
 ($f_s = 30\text{ to }34\text{ kHz}$)

External-bus access isn't supported
 in over 20 MHz.

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (=x)	50	33.3 μ s	62.5		50		ns
2	t_{CLK}	CLK width	2x - 40		85		60		ns
3	t_{AK}	A0 to 23 Valid \rightarrow CLK Hold	0.5x - 20		11		5		ns
4	t_{KA}	CLK Valid \rightarrow A0 to 23 Hold	1.5x - 70		24		5		ns
5	t_{AL}	A0 to 15 Valid \rightarrow ALE fall	0.5x - 15		16		10		ns
6	t_{LA}	ALE fall \rightarrow A0 to 15 Hold	0.5x - 20		11		5		ns
7	t_{LL}	ALE High pulse width	x - 40		23		10		ns
8	t_{LC}	ALE fall \rightarrow $\overline{RD}/\overline{WR}$ fall	0.5x - 25		6		0		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ rise \rightarrow ALE rise	0.5x - 20		11		5		ns
10	t_{ACL}	A0 to 15 Valid \rightarrow $\overline{RD}/\overline{WR}$ fall	x - 25		38		25		ns
11	t_{ACH}	A0 to 23 Valid \rightarrow $\overline{RD}/\overline{WR}$ fall	1.5x - 50		44		25		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ rise \rightarrow A0 to 23 Hold	0.5x - 25		6		0		ns
13	t_{ADL}	A0 to 15 Valid \rightarrow D0 to 15 input		3.0x - 55		133		95	ns
14	t_{ADH}	A0 to 23 Valid \rightarrow D0 to 15 input		3.5x - 65		154		110	ns
15	t_{RD}	\overline{RD} fall \rightarrow D0 to 15 input		2.0x - 60		65		40	ns
16	t_{RR}	\overline{RD} Low pulse width	2.0x - 40		85		60		ns
17	t_{HR}	\overline{RD} rise \rightarrow D0 to 15 Hold	0		0		0		ns
18	t_{RAE}	\overline{RD} rise \rightarrow A0 to 15 output	x - 15		48		35		ns
19	t_{WW}	\overline{WR} Low pulse width	2.0x - 40		85		60		ns
20	t_{DW}	D0 to 15 Valid \rightarrow \overline{WR} rise	2.0x - 55		70		45		ns
21	t_{WD}	\overline{WR} rise \rightarrow D0 to 15 Hold	0.5x - 15		16		10		ns
22	t_{AWH}	A0 to 23 Valid \rightarrow \overline{WAIT} input (1 \overline{WAIT} + n mode)		3.5x - 90		129		85	ns
23	t_{AWL}	A0 to 15 Valid \rightarrow \overline{WAIT} input (1 \overline{WAIT} + n mode)		3.0x - 80		108		70	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ fall \rightarrow \overline{WAIT} Hold (1 \overline{WAIT} + n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0 to 23 Valid \rightarrow PORT input		2.5x - 120		36		5	ns
26	t_{APH2}	A0 to 23 Valid \rightarrow PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	\overline{WR} rise \rightarrow PORT Valid		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V / Low 0.8 V, $CL = 50\text{ pF}$
 (However $CL = 100\text{ pF}$ for AD0 to AD15, A0 to A23, ALE, \overline{RD} , \overline{WR} , \overline{HWR} , R/\overline{W} , CLK)
- Input Level: High 2.4 V / Low 0.45 V (AD0 to AD15)
 High 0.8 V_{CC} / Low 0.2 V_{CC} (Except for AD0 to AD15)

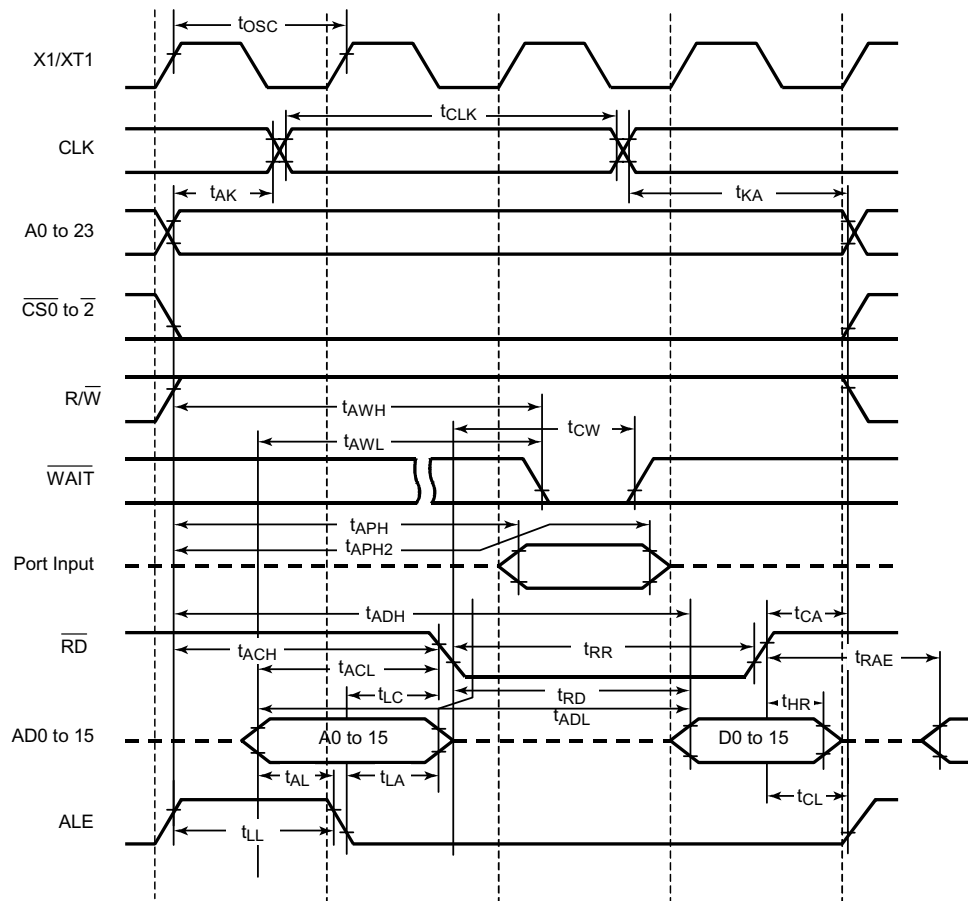
(2) $V_{CC} = 3\text{ V} \pm 10\%$ ($f_c = 4$ to 12.5 MHz)
 ($f_s = 30$ to 34 kHz)

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (=x)	80	33.3 μs	80		ns
2	t_{CLK}	CLK width	2x - 40		120		ns
3	t_{AK}	A0 to 23 Valid \rightarrow CLK Hold	0.5x - 30		10		ns
4	t_{KA}	CLK Valid \rightarrow A0 to 23 Hold	1.5x - 80		40		ns
5	t_{AL}	A0 to 15 Valid \rightarrow ALE fall	0.5x - 35		5		ns
6	t_{LA}	ALE fall \rightarrow A0 to 15 Hold	0.5x - 35		5		ns
7	t_{LL}	ALE High width	x - 60		20		ns
8	t_{LC}	ALE fall \rightarrow \overline{RD} / \overline{WR} fall	0.5x - 35		5		ns
9	t_{CL}	\overline{RD} / \overline{WR} rise \rightarrow ALE rise	0.5x - 40		0		ns
10	t_{ACL}	A0 to 15 Valid \rightarrow \overline{RD} / \overline{WR} fall	x - 50		30		ns
11	t_{ACH}	A0 to 23 Valid \rightarrow \overline{RD} / \overline{WR} fall	1.5x - 50		70		ns
12	t_{CA}	\overline{RD} / \overline{WR} rise \rightarrow A0 to 23 Hold	0.5x - 40		0		ns
13	t_{ADL}	A0 to 15 Valid \rightarrow D0 to 15 input		3.0x - 110		130	ns
14	t_{ADH}	A0 to 23 Valid \rightarrow D0 to 15 input		3.5x - 125		155	ns
15	t_{RD}	\overline{RD} fall \rightarrow D0 to 15 input		2.0x - 115		45	ns
16	t_{RR}	\overline{RD} Low pulse width	2.0x - 40		120		ns
17	t_{HR}	\overline{RD} rise \rightarrow D0 to 15 Hold	0		0		ns
18	t_{RAE}	\overline{RD} rise \rightarrow A0 to 15 output	x - 25		55		ns
19	t_{WW}	\overline{WR} Low pulse width	2.0x - 40		120		ns
20	t_{DW}	D0 to 15 Valid \rightarrow \overline{WR} rise	2.0x - 120		40		ns
21	t_{WD}	\overline{WR} rise \rightarrow D0 to 15 Hold	0.5x - 40		0		ns
22	t_{AWH}	A0 to 23 Valid \rightarrow \overline{WAIT} input (1 \overline{WAIT} + n mode)		3.5x - 130		150	ns
23	t_{AWL}	A0 to 15 Valid \rightarrow \overline{WAIT} input (1 \overline{WAIT} + n mode)		3.0x - 100		140	ns
24	t_{CW}	\overline{RD} / \overline{WR} fall \rightarrow \overline{WAIT} Hold (1 \overline{WAIT} + n mode)	2.0x + 0		160		ns
25	t_{APH}	A0 to 23 Valid \rightarrow PORT input		2.5x - 120		80	ns
26	t_{APH2}	A0 to 23 Valid \rightarrow PORT Hold	2.5x + 50		250		ns
27	t_{CP}	\overline{WR} rise \rightarrow PORT Valid		200		200	ns

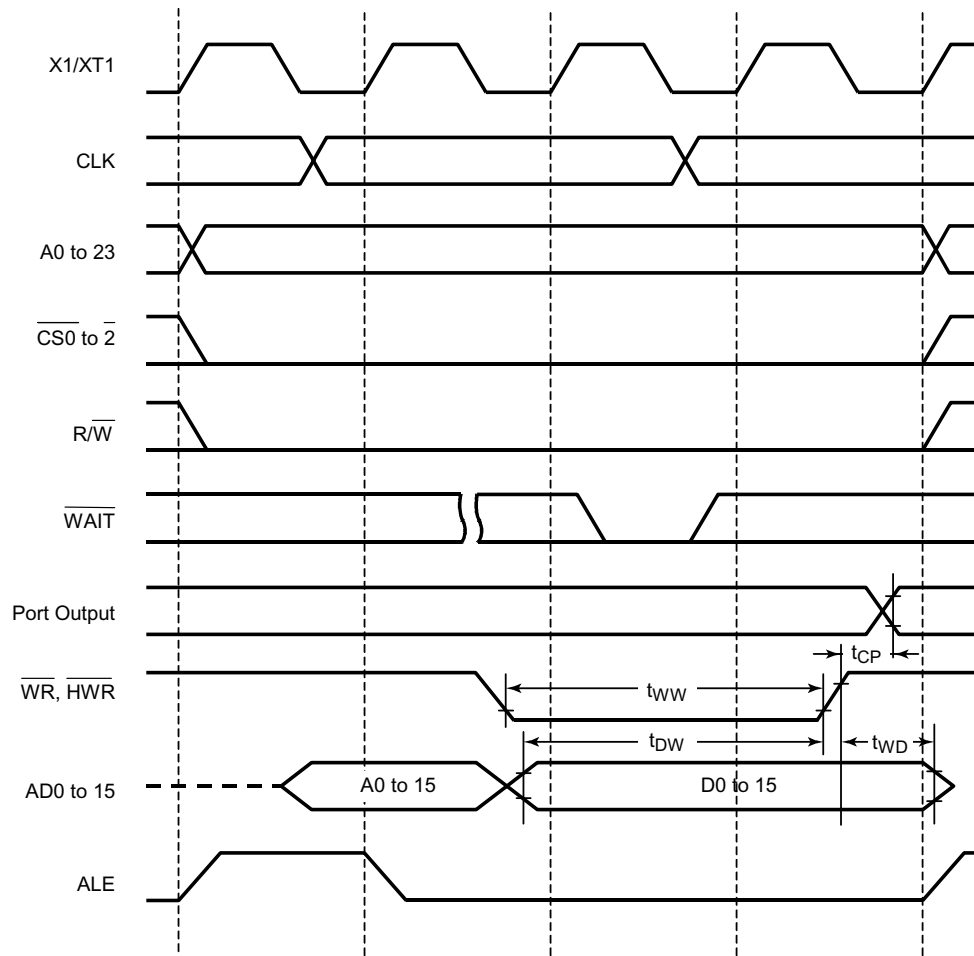
AC Measuring Conditions

- Output Level: High 0.7 V_{CC} / Low 0.3 V_{CC} , $CL = 50\text{ pF}$
- Input Level: High 0.9 V_{CC} / Low 0.1 V_{CC}

(1) Read Cycle



(2) Write Cycle



4.4 AD Conversion Characteristics ($V_{SS} = 0\text{ V}$, $AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$)

 $V_{CC} = +5\text{ V} \pm 10\%$, ($f_c = 4\text{ to }25\text{ MHz}$)

 $V_{CC} = +3\text{ V} \pm 10\%$, ($f_c = 4\text{ to }12.5\text{ MHz}$)

Parameter		Symbol	TestConditions	Min	Typ.	Max	Unit
AD analog reference supply voltage (+)		V_{REFH}		$V_{CC} - 0.2$		V_{CC}	V
AD analog reference supply voltage (-)		V_{REFL}		V_{SS}		$V_{SS} + 0.2$	
Analog reference voltage		AV_{CC}		$V_{CC} - 0.2$		V_{CC}	
Analog reference voltage		AV_{SS}		V_{SS}		$V_{SS} + 0.2$	
Analog input voltage		V_{AIN}		V_{REFL}		V_{REFH}	
Analog input impedance		R_{AIN}				5	k Ω
Analog reference voltage supply current	$\langle V_{REFON} \rangle = 1$	I_{REF}	$V_{CC} = 5\text{ V} \pm 10\%$			3.7	mA
			$V_{CC} = 3\text{ V} \pm 10\%$			2.2	
	$\langle V_{REFON} \rangle = 0$		$V_{CC} = 2.7\text{ to }5.5\text{ V}$		0.02		5.0
Total tolerance (excludes quantization error)		E_T	$V_{CC} = 5\text{ V} \pm 10\%$			± 3	LSB
			$V_{CC} = 3\text{ V} \pm 10\%$			± 3	

Note 1: $1\text{LSB} = (V_{REFH} - V_{REFL})/210[V]$

Note 2: Power supply current I_{CC} from the VCC pin includes the power supply current from the AVCC pin.

4.5 Serial Channel Timing (Serial channel 2, 3 and 4)

(1) SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	16X		488 μs		1.28 μs		0.8 μs	
Output Data \rightarrow Rising edge of SCLK	t_{OSS}	$t_{SCY}/2 - 5X - 50$		91.5 μs		190 ns		100 ns	
SCLK edge* \rightarrow Output Data hold	t_{OHS}	5X - 100		152 μs		300 ns		150 ns	
SCLK edge* \rightarrow Input Data hold	t_{HSR}	0		0		0		0	
SCLK edge* \rightarrow effective data input	t_{SRD}		$t_{SCY} - 5X - 100$		336 μs		780 ns		450 ns

* It is rising edge in using rising edge mode and falling edge in using falling edge mode.

(2) SCLK Output Mode

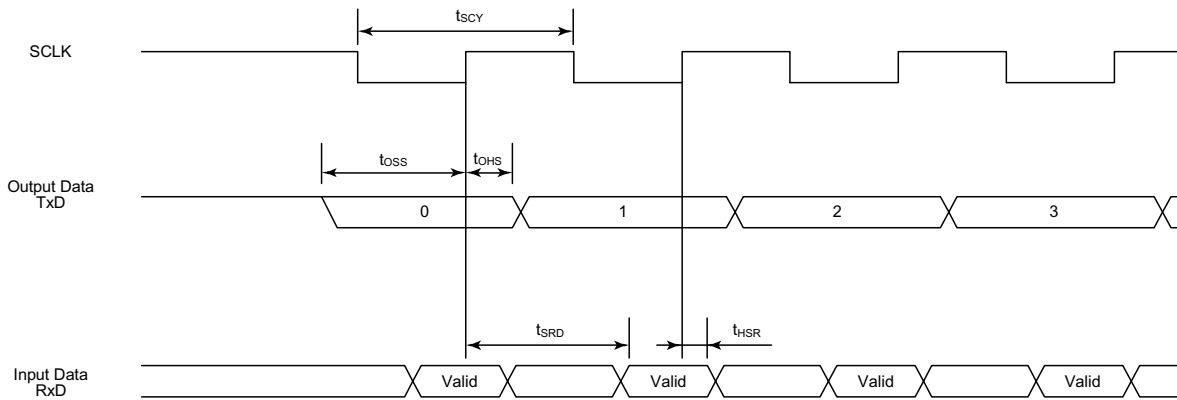
Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28 μs	655.36 μs	0.8 μs	409.6 μs
Output Data \rightarrow SCLK rising edge	t_{OSS}	$t_{SCY} - 2X - 150$		427 μs		970 ns		550 ns	
SCLK rising edge \rightarrow Output Data hold	t_{OHS}	2X - 80		60 μs		80 ns		20 ns	
SCLK rising edge \rightarrow Input Data hold	t_{HSR}	0		0		0		0	
SCLK rising edge \rightarrow effective data input	t_{SRD}		$t_{SCY} - 2X - 150$		428 μs		970 ns		550 ns

(3) SCLK Input Mode (UART mode)

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	$4X + 20$		122 μ s		340 ns		220 ns	
Low level SCLK Pulse width	t_{SCYL}	$2X + 5$		6 μ s		165 ns		105 ns	
High level SCLK Pulse width	t_{SCYH}	$2X + 5$		6 μ s		165 ns		105 ns	

Note: fs is used as system clock or input clock to prescaler.

Timing Chart for I/O Interface Mode



Note: SCLK is reversed in SCLK input falling mode.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	$8X + 100$		740		500		ns
Low level pulse width	t_{VCKL}	$4X + 40$		360		240		ns
High level pulse width	t_{VCKH}	$4X + 40$		360		240		ns

4.7 Interrupt and Capture

(1) \overline{NMI} , INT0 interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
\overline{NMI} , INT0 Low level pulse width	t_{INTAL}	$4X$		320		200		ns
\overline{NMI} , INT0 High level pulse width	t_{INTAH}	$4X$		320		200		ns

(2) INT4 to 7

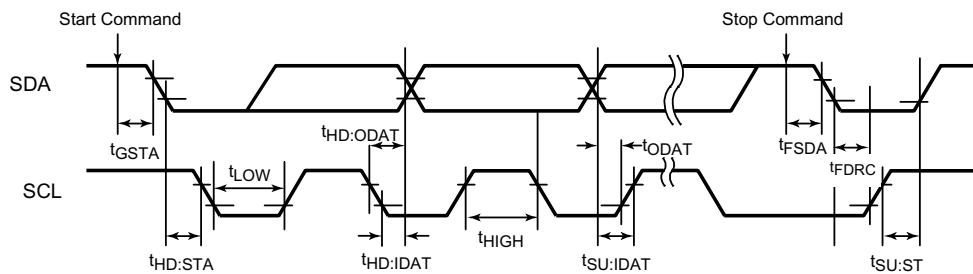
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT4 to INT7 Low level pulse width	t_{INTBL}	$4X + 100$		420		300		ns
INT4 to INT7 High level pulse width	t_{INTBH}	$4X + 100$		420		300		ns

4.8 Serial Bus Interface Timing

(1) I²C bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ	Max	
START command → SDA fall	t_{GSTA}	$3X$			s
Hold time START condition	$t_{HD:STA}$	2^nX			s
SCL Low level pulse width	t_{LOW}	2^nX			s
SCL High level pulse width	t_{HIGH}	$2^nX + 8X$			s
Data hold time (input)	$t_{HD:IDAT}$	0			ns
Data set-up time (input)	$t_{SU:IDAT}$	250			ns
Data hold time (output)	$t_{HD:ODAT}$	$7X$		$11X$	s
Data output → SCL Rising edge	t_{ODAT}		$2^nX - t_{HD:ODAT}$		s
STOP command → SDA falling edge	t_{FSDA}	$3X$			s
SDA Falling edge → SCL Rising edge	t_{FDRC}	2^nX			s
Set-up time STOP condition	$t_{SU:STO}$	$2^nX + 16X$			s

Note: "n" value is set by SBICR1 <SCK2 to 0>



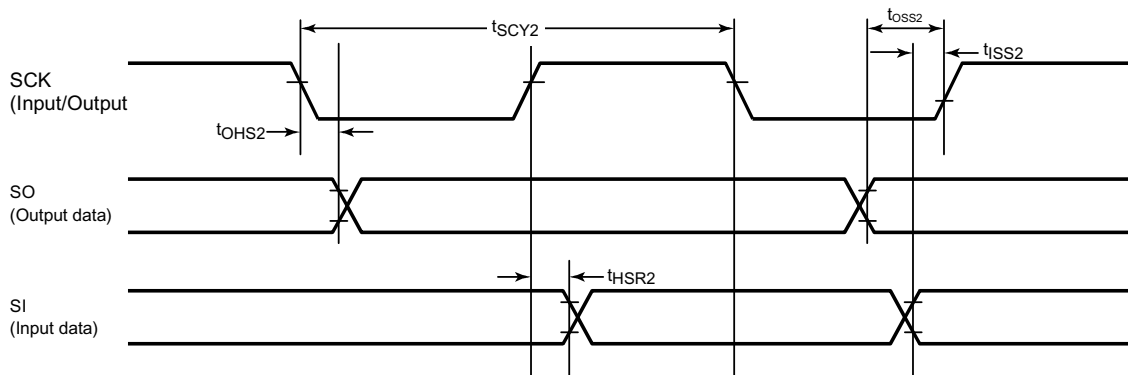
(2) Clocked-synchronous 8-bit SIO Mode

a. SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling edge → Output data hold	t_{OHS2}	$6X$		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 6X$	s
SCK rising edge → Input data hold	t_{HSR2}	$6X$		ns
Input data → SCK rising edge	t_{ISS2}	0		ns

b. SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling edge → Output data hold	t_{OHS2}	$2X$		s
Output data → SCK rising edge	t_{OSS2}		$t_{SCY2}/2 - 2X$	s
SCK rising edge → Input data hold	t_{HSR2}	$2X$		s
Input data → SCK rising edge	t_{ISS2}	0		ns



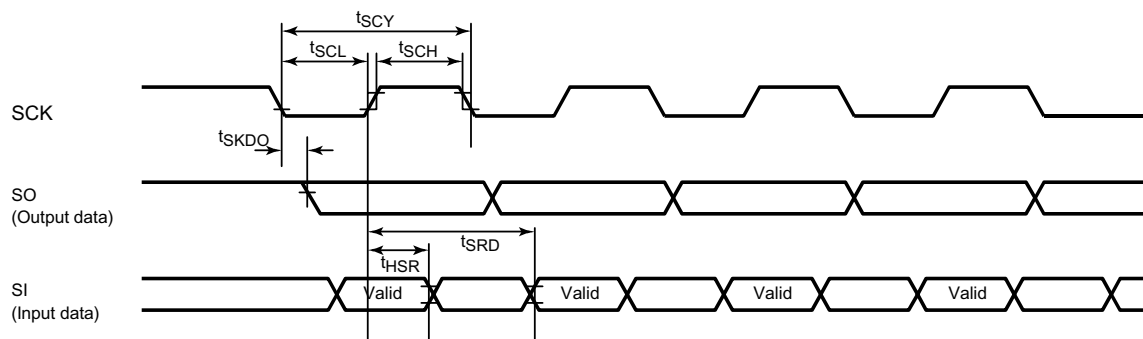
4.9 Timing Chart for Serial Channel 0,1

a. SCK input mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	6X		ns
SCK rising edge → Effective data input	t_{SRD}		$t_{SCY} - 2X$	ns
SCK rising edge → Input data hold	t_{HSR}	6X		ns

b. SCK output mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK cycle	t_{SCY}	16X		ns
SCK falling edge → Output data hold	t_{SKDO}	2X		ns
SCK rising edge → Effective data input	t_{SRD}		$t_{SCY} - 2X$	ns
SCK rising edge → Input data hold	t_{HSR}	2X		ns

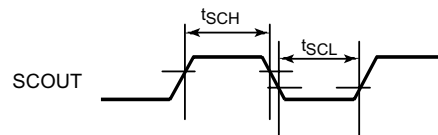


4.10 SCOUT pin AC characteristics

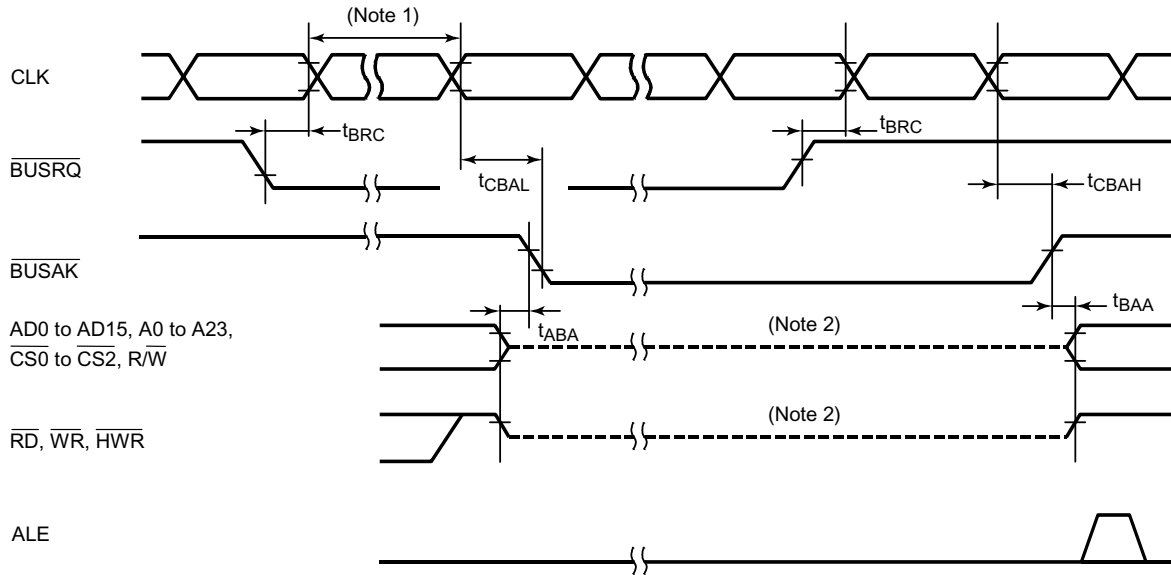
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max		Min	Max	Min	
High-level pulse width VCC = 5 V ± 10%	t_{SCH}	0.5X - 10			30	15		ns
VCC = 3 V ± 10%		0.5X - 20			20	—	—	ns
Low-level pulse width VCC = 5 V ± 10%	t_{SCL}	0.5X - 10			30	15		ns
VCC = 3 V ± 10%		0.5X - 20			20	—	—	ns

Measurement condition

Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.11 Timing Chart for Bus Request ($\overline{\text{BUSRQ}}$) / Bus Acknowledge ($\overline{\text{BUSAK}}$)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{BUSRQ}}$ set-up time to CLK	t_{BRC}	120		120		120		ns
CLK → $\overline{\text{BUSAK}}$ falling edge	t_{CBAL}		$1.5X + 120$		240		195	ns
CLK → $\overline{\text{BUSAK}}$ rising edge	t_{CBAH}		$0.5X + 40$		80		65	ns
Output Buffer is off to $\overline{\text{BUSAK}}$ falling edge	t_{ABA}	0	80	0	80	0	80	ns
$\overline{\text{BUSAK}}$ rising edge to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1: The Bus will be released after the $\overline{\text{WAIT}}$ request is inactive, when the $\overline{\text{BUSRQ}}$ is set to 0 during Wait cycle.

Note 2: This line shows the output buffer is off-state. It doesn't indicate the signal level is fixed.

Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level - fix will be delayed.

The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

4.12 Read operation in PROM mode

DC/AC characteristics

 $T_a = 25 \pm 5^\circ\text{C}$ $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}	—	4.5	5.5	V
Input High Voltage (A0 to A16, \overline{CE} , \overline{OE} , \overline{PGM})	V_{IH1}	—	2.2	$V_{CC} + 0.3$	V
Input Low Voltage (A0 to A16, \overline{CE} , \overline{OE} , \overline{PGM})	V_{IL1}	—	-0.3	0.8	V
Address to Output Delay	t_{ACC}	$C_L = 50\text{ pF}$	—	$2.25TCYC + \alpha$	ns

TCYC = 400 ns (10 MHz Clock)

 $\alpha = 200\text{ ns}$

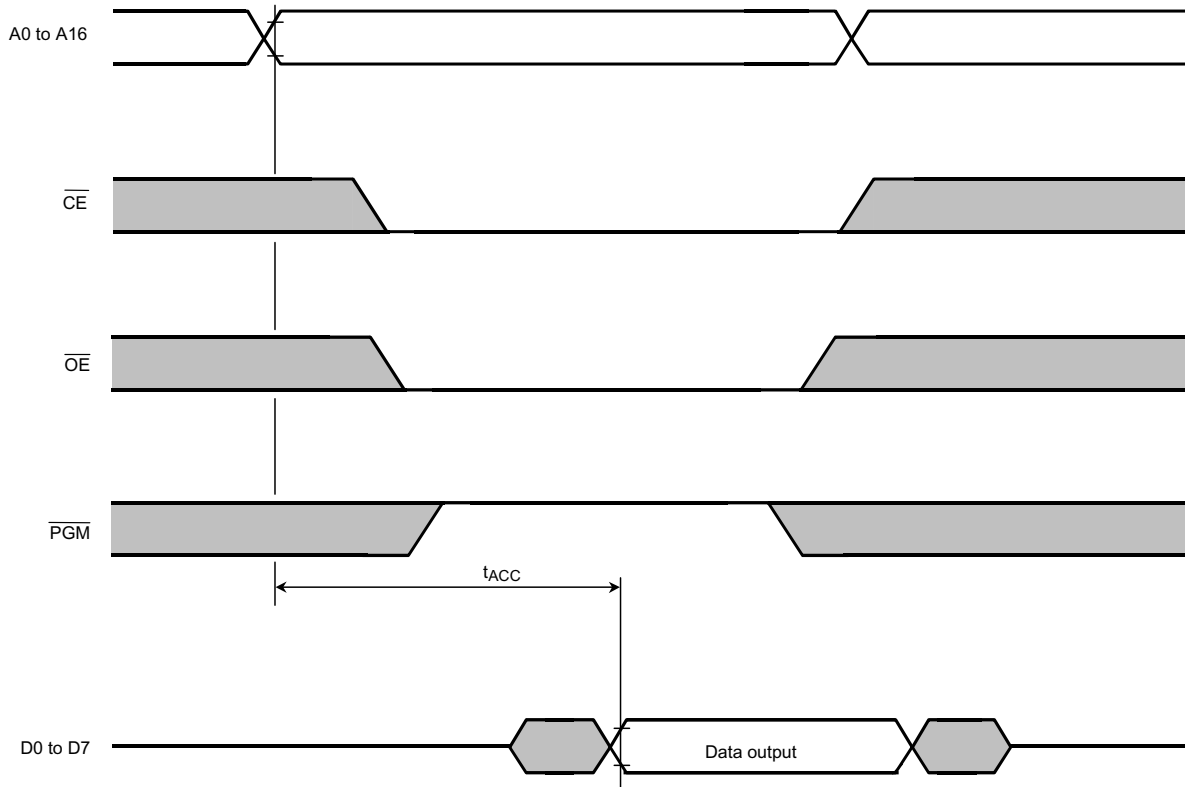
4.13 Program operation in PROM mode

DC/AC characteristics

 $T_a = 25 \pm 5^\circ\text{C}$ $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$

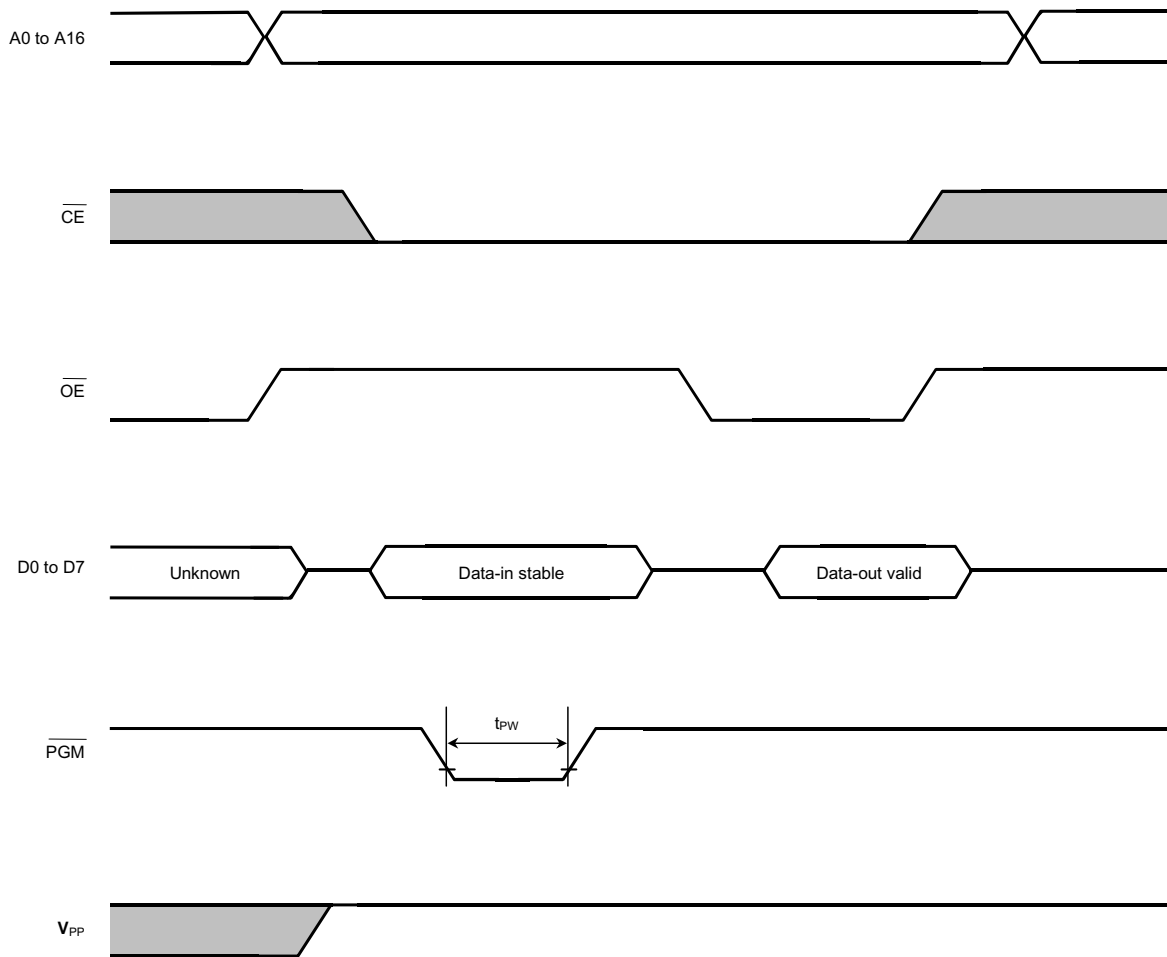
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programming Supply Voltage	V_{PP}	—	12.50	12.75	13.00	V
Input High Voltage (D0 to D7, A0 to A16, \overline{CE} , \overline{OE} , \overline{PGM})	V_{IH}	—	2.6		$V_{CC} + 0.3$	V
Input Low Voltage (D0 to D7, A0 to A16, \overline{CE} , \overline{OE} , \overline{PGM})	V_{IL}	—	-0.3		0.8	V
V_{CC} Supply Current	I_{CC}	$f_c = 10\text{ MHz}$	—		50	mA
V_{PP} Supply Current	I_{PP}	$V_{PP} = 13.00\text{ V}$	—		50	mA
\overline{PGM} Program Pulse Width	t_{PW}	$C_L = 50\text{ pF}$	0.095	0.1	0.105	ms

4.14 Timing chart of read operation in PROM mode



4.15 Timing chart of program operation in PROM mode

High-Speed Programming formula



Note 1: The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC} .

Note 2: The pulling up/down device on condition of $V_{PP} = 12.75$ V suffers a damage for the device.

Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be careful a overshoot at the programming.